IN THE CLAIMS:

Claim 1 (currently amended) A semiconductor device, comprising:

an I/O region formed on a chip and having at least an input/output pad;

a plurality of active regions formed on said chip, said active regions being separated from one another by a boundary region;

a plurality of logic circuits having either one of the same functions and different functions being mounted in each of said active regions, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits;

wherein each of said plurality of mounted logic circuits is operated by setting an SEL signal for selectively turning a plurality of ~~transistor~~ transistors on and off for each of said mounted logic circuits, to one of a high and a low level.

Claim 2 (previously presented) A semiconductor device comprising:

an I/O region formed on a chip and having at least an input/output pad;

an active region formed on said chip;

a plurality of logic circuits having either one of the same functions and different functions being mounted in said active region, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits;

wherein said selection circuit includes a buffer circuit having a disconnecting section, said buffer circuit being substantially free of transistors and inverters, and said disconnecting section being disconnected to allow permanent setting of an operable circuit.

Claim 3 (original) The semiconductor device according to claim 2, wherein said disconnecting section includes a fuse.

Claim 4 (previously presented) The semiconductor device according to claim 1, wherein said selection circuit selects a logic circuit to be operated on a basis of a signal input supplied through said input/output pad.

Claim 5 (previously presented) A semiconductor device comprising:

an I/O region formed on a chip and having at least an input/output pad;

an active region formed on said chip;

a plurality of logic circuits having either one of the same functions and different functions being mounted in said active region, and

a selection circuit for selectively operating only one of said plurality of mounted logic circuits;

wherein said selection circuit includes a transistor element connected in series with each said logic circuit between said logic circuit and a power terminal, and

said transistor element selects a logic circuit to be operated on a basis of a signal input supplied through said input/output pad.